What is claimed is:

[Claim 1] 1. A method of initializing a plurality of processors in an integrated circuit, the method comprising the steps of:

identifying each one of the processors;

executing boot code for initializing each one of the processors, the boot code containing specific code for at least one of the processors and common code that is common for each one of the processors, the specific code being accessed according to the identity of the processor executing the boot code.

[Claim 2] 2. The method of claim 1 wherein the step of identifying includes the step of:

assigning a unique value to each one of the processors.

[Claim 3] 3. The method of claim 2 wherein each one of the processors includes a register and the step of assigning includes the step of:

providing a unique value to the register of the processor.

[Claim 4] 4. An apparatus for initializing a plurality of processors in an integrated circuit, the apparatus comprising:

means for identifying each one of the processors;

means for executing boot code for initializing each one of the processors, the boot code containing specific code for at least one of the processors and common code that is common for each one of the processors, the specific code being accessed according to the identity of the processor executing the boot code.

[Claim 5] 5. The apparatus of claim 4 wherein the means for identifying includes:

means for assigning a unique value to each one of the processors.

[Claim 6] 6. The apparatus of claim 5 wherein each one of the processors includes a register and the means for assigning includes:

means for providing a unique value to the register of the processor.

[Claim 7] 7. An integrated circuit comprising:

a plurality of processors each having a unique identifier;

a bus for providing data to and from each one of the processors;

a memory, coupled to the bus, having boot code for initializing each one of the processors, the boot code using the unique identifier of each processor to access code that is unique to the identified processor.

[Claim 8] 8. The integrated circuit of claim 7 wherein each one of the processors has at least one register, and the at least one register is used to store a unique identifier.

[Claim 9] 9. The integrated circuit of claim 7 further comprising a cache shared between the plurality of processors.

[Claim 10] 10. A method of initializing multiple processors in an integrated circuit, the method comprising the steps of:

creating boot code for initializing the processors, the boot code having code that is common for each one of the processors, and code that is specific for each one of the processors;

assigning each one of the processors a unique identifier; and

executing the boot code and accessing code that is specific for a processor using the unique identifier of the processor.

[Claim 11] 11. The method of claim 10 wherein the step of assigning includes the step of:

storing a unique value into a register of each one of the processors.